

Optical Transceivers for 100 Gigabit Ethernet and its Transport

Jon Anderson and Matthew Traverso, Opnext, Inc.

ABSTRACT

A new generation of optical transceivers for 100 Gigabit Ethernet client interconnection and line system transmission are now being developed and deployed for data center and transport applications. This article provides an overview and status of the 100 G Form-factor Pluggable Multi-Source Agreement for client applications and the Optical Internetworking Forum 100 G Transponder Module Implementation Agreement for long distance DWDM transmission applications.

INTRODUCTION

Data center and commercial network operators have cited the need for 100 Gigabit Ethernet (GbE) connectivity and transport to support ever increasing internet traffic growth over the next decade. Responding to this demand, the IEEE 802.3 Working Group (WG) and ITU-T Study Group (SG) 15 have recently reached milestones in standards development of specifications for supporting 100GbE client interfaces [1] and transmission across Optical Transport Network (OTN)-based core transport networks [2]. With these draft standards now established, system, sub-system, module and component vendors are working in industry consortia towards developing a new generation of optical transceivers for 100GbE client interconnection and line system transmission, with the anticipation of initial deployment in the 2010–2011 time frame. This article provides an overview and status of the 100 G Form-factor Pluggable Multi-Source Agreement (CFP MSA) for client applications and the Optical Internetworking Forum (OIF) 100 G Transponder Module Implementation Agreement (100 G Module IA) for long distance Dense Wavelength Division Multiplexing (DWDM) transmission applications.

100GBE CLIENT APPLICATION

The IEEE P802.3ba WG has nearly completed their work on the standardization of 100GbE. The standard provides documentation both on the structure and mapping of data to be compliant with 100GbE and also on physical interfaces (Table 1). The proposed interfaces span copper media of 7 m, to multi-mode fiber media of 100 m, to single mode fiber media up to 40 km, and

all use parallel bit streams. The copper applications specify ten lanes each operating at 10 Gb/s transmitted over ten copper pairs for each direction assembled into a single cable. The multi-mode fiber applications specify ten lanes each operating at 10 Gb/s transmitted over ten individual fibers for each direction typically assembled into a single cable. The single mode fiber applications specify four lanes at 25 Gb/s transmitted over a single duplex fiber at four different wavelengths.

In addition to these physical layer interfaces, the IEEE P802.3ba WG has specified optional interfaces for within a 100GbE system, linking *chip to chip* or *chip to module*. The CPPI (100 Gigabit Parallel Physical Interface) is a chip to module interface specified to eliminate the need for clock and data recovery circuits within the module. The CAUI (100 Gigabit Attachment Unit Interface) is both a chip to chip and a chip to module interface. CAUI is specified to require the use of clock and data recovery circuits and as such allows for longer and noisier transmission channels than those used for CPPI.

CFP MSA

The industry has been developing a few module form factors to support the IEEE P802.3ba draft interfaces. Module form factors such as the CFP MSA [3] allow systems designers to speed up their design cycle, saving time and resources versus implementing a design with discrete components. Additionally, the definition of the CFP MSA slot creates a single system configuration which can be easily adapted to accommodate different reach and optical interface types.

The CFP MSA has defined a module form factor which emphasizes flexibility with multiple pin-map configurations ranging from three interfaces of XLAUI (40 Gigabit Attachment Unit Interface) to a single OTL4.10 (Optical channel Transport Lane level 4) interface. The pin-map flexibility leverages the current industry common denominator lane rate of 10 Gb/s. This common lane rate simplifies the design of network system ASICs to interface to CFP and other modules for 100GbE applications. The electrical interface specified for 100GbE applications is CAUI.

Shown in the block diagram in Fig. 1 is a generic picture of the common components contained within a CFP MSA module. The interface IC(s) for 100 GBASE-LR4 and 100 GBASE-ER4 applications support a gearbox functionality

PMD support	100 Gigabit Ethernet
Copper cable (at least 7 m)	100GBASE-CR10
Multi-mode fiber (at least 100 m)	100GBASE-SR10
Single mode fiber (at least 10 km)	100GBASE-LR4
Single mode fiber (at least 40 km)	100GBASE-ER4

Table 1. Proposed interfaces.

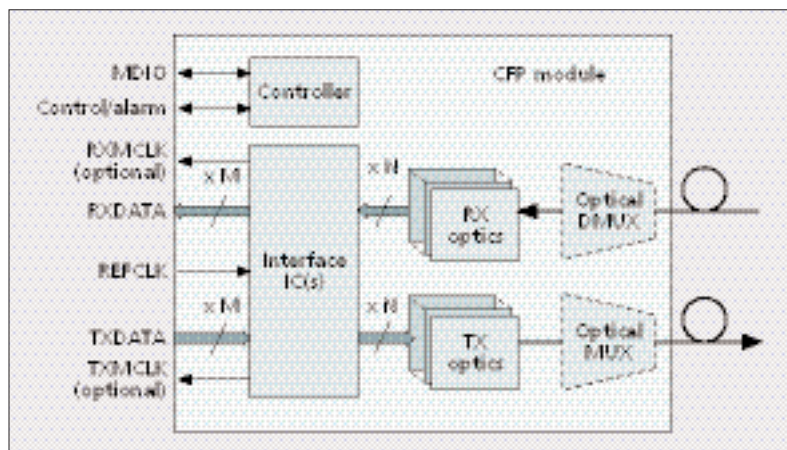


Figure 1. CFP MSA block diagram.

to transition from the CAUI lane mapping of ten lanes operating at a nominal rate of 10 Gb/s to four lanes operating at a nominal rate of 25 Gb/s. The transmitter optical specifications for 100 GBASE-LR4 and 100 GBASE-ER4 were based upon Electro-Absorption Distributed FeedBack (EA-DFB) laser technology, but were written to allow for eventual implementation with directly modulated lasers such as DFBs. The receiver optical specifications for 100 GBASE-LR4 and 100 GBASE-ER4 were based upon Positive-Intrinsic-Negative PhotoDiode (PIN-PDs) detector technology. In the development of the IEEE P802.3ba 100 GBASE-ER4 specification the receiver was assumed to include optical amplification such as a Semiconductor Optical Amplifier (SOA) to compensate for the optical loss budget of 40 km of single mode fiber.

PLUGGABLE CONNECTOR

The CFP MSA is defined to be hot pluggable allowing the CFP MSA module to be inserted into a 100GbE system without any need for the system to be shut down. Some previous pluggable modules for optical networking applications have also supported hot pluggability. Historically, the primary challenge has been limiting the inrush current into a hot pluggable module without causing a brown out condition to other components within the system.

However, the expected high power dissipation

of 100 GBASE-LR4 and 100 GBASE-ER4 places unique challenges upon both the module and the system for inrush current. The highest power class of the CFP MSA supports a power dissipation of 32 W which corresponds to a current of 10 A since the CFP MSA only requires a single power supply of 3.3 V. In order to limit opportunities for current arcing the CFP electrical connector has different contact lengths such that the order of contact pin engagement is fixed. Via a *Module Absent* contact pin which has the shortest length, the host is able to detect the moment when the module is extracted. Via a *Module Low Power* contact pin which also has the shortest length, the module is able to detect the moment when the module is extracted. The CFP MSA module supports a rapid turn off procedure to allow for the module to be unplugged without risk of electrical arcing.

The CFP MSA uses a two piece electrical connector system. The 100GbE system contains a CFP MSA receptacle connector which is similar to devices used for various 10 GbE form factors. However, the CFP MSA receptacle connector controls the pin contacts and dictates the order of pin contact engagement of the module as described in the case of the Module Absent and Module Low Power pins. The module plug connector is a different concept than used in previous form factors which used the edge of the module Printed Circuit Board (PCB). The module plug connector is built into the CFP MSA module and has fixed mechanical dimensions. Previously module PCB thickness would determine the insertion and extraction force, but with the module plug connector the constraints on the module PCB thickness are reduced. Additionally, the two piece electrical connector allows for more controlled tolerancing on the electrical mating. The more tightly controlled electrical mating improves the signal integrity performance of the CFP MSA connector.

MODULE SIZE

One of the motivations for transitioning to a higher speed networking interface is to maintain or increase system density. There are many parameters which limit the overall system density including:

- Power dissipation
- Module height & width
- Module length
- IC switching capacity
- IC electrical interface

Graphed in Fig. 2 is an example of some pluggable form factors used for 10 GbE and the CFP MSA for 100GbE plotted according to the publication of each form factor. The y-axis represents the effective faceplate area used by the module divided by the supported data rate. As shown in the graph, the CFP MSA supports slightly higher faceplate density than SFP+, the fourth generation 10 GbE form factor, when considering the relative data rate of each.

However, early generation CFP MSA modules will likely have higher power dissipation due to the emerging nature of the components used for 100GbE. Thus overall system density is likely to initially be limited by thermal constraints on power dissipation. Additionally, the length of the

CFP MSA module is much longer than many of the 10 GbE form factors. The increased length supports high power dissipation by increasing the module surface area.

Not shown in the graph below are the common 10 G and 40 G 300-pin MSA form factors. These form factors were designed primarily for SONET and SDH applications, but some early 10 GbE systems were constructed using the 10 G 300-pin MSA form factor. For the 300-pin MSA, the modules are mounted onto the host system during system construction and the modules are not intended to be accessible to the end user or technician. For 100GbE, the CFP MSA has enabled the industry to skip over this interim step of board mountable only form factors directly to a pluggable interface.

CFP MSA MANAGEMENT INTERFACE

The CFP MSA defined a management interface based upon the IEEE Management Data Input/Output/Management Data Clock (MDIO/MDC) interface ([1], Clause 45). The CFP MSA includes several new features enabled by the management interface: programmable controls and alarms, module state transitions, and error rate calculations.

The CFP MSA defines several different module functional states to allow the 100GbE hosts to actively control the behavior of the module (Fig. 3). There are two types of states defined: steady state and transient state.

The steady states represent stable operating conditions for the CFP MSA module such as the Low Power State, TX-Off State, and the Ready State. The clear definition of such states simplifies debugging and operation of the CFP module within the 100GbE system.

100GbE TRANSPORT APPLICATION

In considering the long-term trend of traffic growth and evolution requirements for long distance transport in high capacity core optical networks, the OIF has developed a framework [4] that identifies target system objectives, technology building blocks and optical transceiver functional architecture for 100 G DWDM long distance transmission. This framework has been used to guide detailed work in the OIF on implementation of 100 G optical transceivers that includes modulation format, coherent detection, Forward Error Correction (FEC) considerations, electro-mechanicals and management interface. While the OIF 100 G optical transceiver implementation strives to be generic for 100 G transmission, 100GbE is the key client payload motivating the transceiver specification. ITU-T SG 15 has been working closely with IEEE 802.3 WG towards specification of a new transmission rate and signal format to accommodate transport of the 100GbE signal across the OTN. Specifically, the Optical channel Transport Unit level 4 (OTU4) has recently been defined and adopted in ITU-T Rec. G.709 Amendment 3 [2]. The OIF has assumed the OTU4 signal as the base rate and format in its specification of the electrical interface between the optical transceiver and the host system framing device.

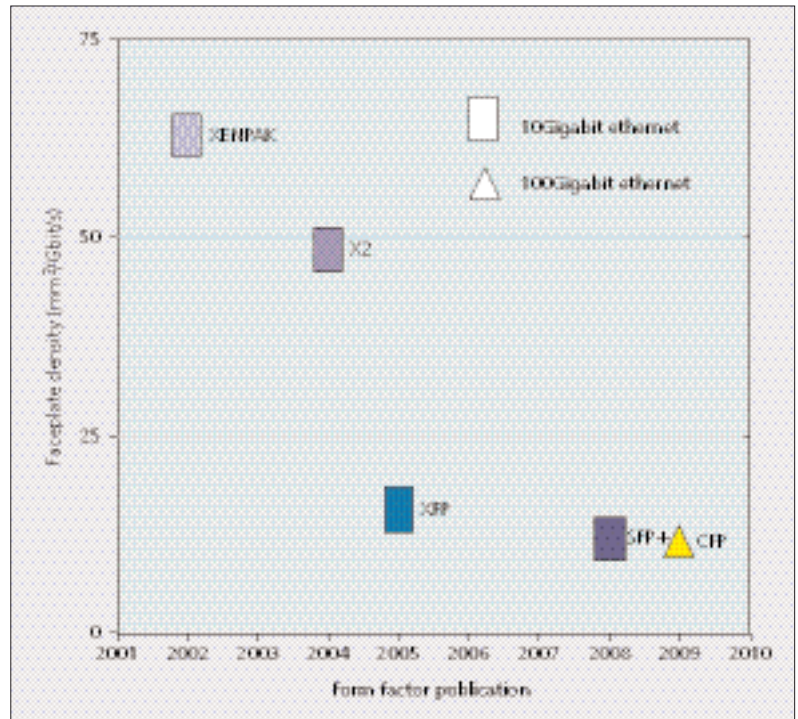


Figure 2. Graph of pluggable form factors according to the faceplate aperture and module pitch versus the publication of the form factor specification.

TX/RX INTEGRATED PHOTONICS TECHNOLOGIES

The OIF framework adopted dual polarization quadrature phase shift keying (DP-QPSK) modulation with coherent detection for specifying the optical transmitter and receiver designs in the 100 G optical transceiver. The DP-QPSK modulation format was determined to better meet target 100 G transmission objectives in comparison to other modulation formats. Dual polarization enables the modulation rate necessary for a 100 G signal to be reduced by a factor of two, thus reducing the required optical bandwidth, which in turn allows for more tightly spaced channels in the DWDM grid, namely maintaining a 50 GHz channel spacing for 100 G signals. QPSK enables the transmitted symbol rate to be reduced by a factor of two which reduces the speed required of opto-electronic components in 100 G transmission. In combination, DP and QPSK reduce the required symbol rate by a factor of four, thus enabling lower cost opto-electronic technologies to be utilized for 100 G transmission. In addition, the lower symbol rates reduces the sensitivity of the 100 G signal to optical propagation impairments, such as chromatic and polarization mode dispersion, and increases noise tolerance to sources such as amplified spontaneous emission (ASE) generated by in-line optical amplifiers.

For the 100 G optical receiver, a coherent detection approach was adopted by the OIF, primarily due to its improved optical signal noise ratio (OSNR) and propagation impairment compensation in comparison to other approaches. With a coherent optical receiver, the phase information of the received optical signal is preserved and both polarizations can be recovered by high-speed electronic equalization.

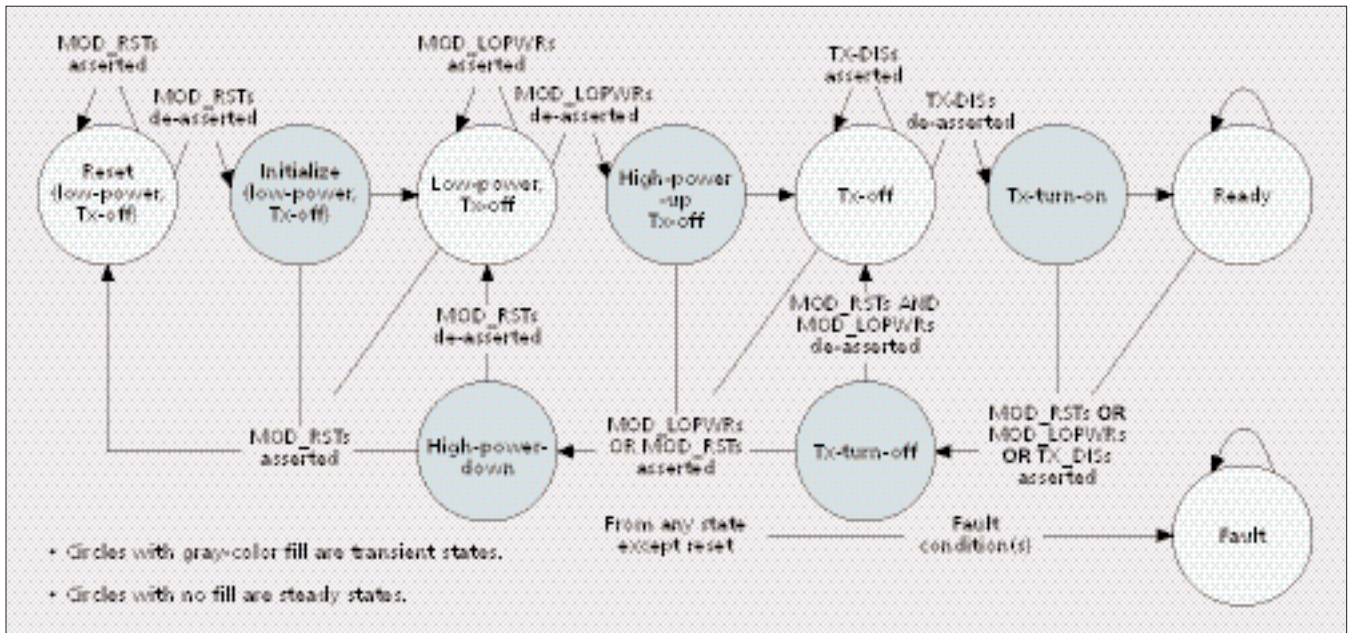


Figure 3. CFP MSA start-up simplified flow diagram.

DP-QPSK modulation requires a highly complex design of numerous passive and active optical, electrical, and opto-electrical components as well as extensive signal processing for performing optical impairment mitigation. Implementation of this design, however, may now be economically feasible through the use of:

- Standardized optical components based on integrated photonic technologies, such as silicon based photonic waveguides, micro-fabrication, and hybrid assembly techniques
- Digital signal processor (DSP) ASIC with high-speed analog-to-digital converters (ADC) enabling optical impairment mitigation to be performed in the digital domain rather than the optical domain

The functional architecture of a DP-QPSK transmitter is illustrated in Fig. 4. The Integrated Polarization Multiplexed Quadrature (PM-Q) Modulator is identified in Fig. 4 and is the subject of detailed implementation agreement work in the OIF. This work includes specification of optical, electrical and electro-optical properties,

electrical interface pin-out and mechanical details. For the transmitter design, a continuous wave (CW) laser source output is split by a beam splitter (BS) into two components (X, Y) with each component independently modulated by a quadrature modulator. The CW laser source is not specified by OIF, but is vendor specified and is typically required to be compliant with ITU-T Recommendation “G.959.1 Optical Transport Network Physical Layer Interfaces” (Nov. 2009). The quadrature modulator is generically composed of two nested Mach-Zehnder modulators with bias control, a 90° phase shifter with phase control, and a monitoring photodiode (MPD) for output optical power monitoring. Modulator drivers and associated electronics for in-phase (I) and quadrature (Q) high-speed data encoding, I/Q bias control, phase control and optical power control are external to the PM-Q modulator. The modulated signals are re-combined by a beam combiner (BC) with their polarizations orthogonal to each other and transmitted on an output optical fiber. The PM-Q modulator is

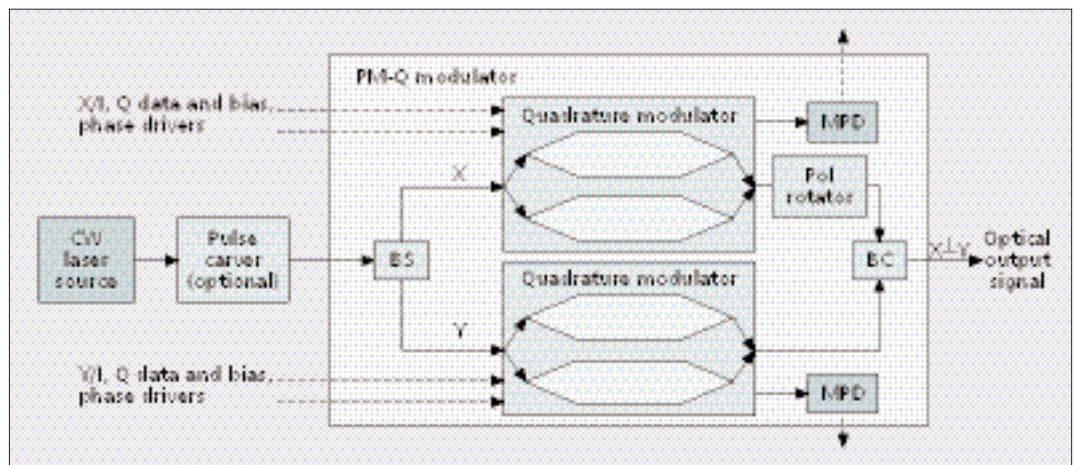


Figure 4. Functional architecture of a 32 GBaud DP-QPSK transmitter with a detailed PM-Q modulator.

specified to provide a minimum bandwidth of 23 GHz for supporting applications with nominal symbol rates of up to 32Gbaud.

The functional architecture of a DP-QPSK receiver is illustrated in Fig. 5. The Integrated Dual Polarization Intradyned Coherent Receiver is identified in Fig. 5 and is also the subject of detailed implementation agreement work in the OIF. This work includes specification of optical, electrical and electro-optical properties, electrical interface pin-out, and mechanical details. For the coherent receiver design, a polarization beam splitter (PBS) is used to split the received optical signal (from a DP-QPSK transmitter) into two components (X, Y) with orthogonal polarizations. These polarized optical signals are mixed with a local oscillator laser source at a frequency near that of the received optical signal, generating mixing products at the difference frequency. The resultant analog products are down converted, detected electronically, linearly amplified, digitized in high-speed ADCs and then passed to a DSP ASIC chip set. The DSP ASIC chip set functionality and interface specifications are vendor specified and not specified by the OIF. However, the DSP ASIC chip set most likely will include equalization functionality for propagation impairment compensation and high-speed electrical Serialization-Deserialization (SerDes) interface functionality. The DP coherent receiver and local oscillator are specified to provide a typical bandwidth of 22 GHz for supporting applications on the ITU-T Rec. G.694.1 50 GHz grid with symbol rates up to 32 Gbaud.

100 G TRANSCEIVER ARCHITECTURE

The OIF is also working on implementation specifications of an optical transceiver for supporting 32Gbaud long distance DWDM transmission. These specifications specifically address module electro-mechanical and management interface aspects. While the optical transceiver module specifications specifically incorporate the DP-QPSK transmitter and receiver integrated photonics technologies described above, these specifications strive to be modulation format and data rate agnostic so as to maximize applicability to future market applications.

The functional architecture of the 32Gbaud optical transceiver is illustrated in Fig. 6. Major module functions include transmitter and receiver optics, such as the DP-QPSK transmitter and DP intradyne coherent receiver described above, modulation drivers, ADCs and receiver DSP, electrical interface IC for adapting the host system signals frame format to the optical modulation format, a controller supporting an MDIO/MDC management interface, and power conversion and filtering of a single +12 V DC power supply from the host system. The 100 G optical transceiver is not designed to be hot pluggable as is the CFP module, but rather is fixed to the system host board. A 168-pin two-row electrical connector is specified in the OIF 100 G Module IA to support the electrical interface between the transceiver module and the host system line card. The hardware pin functionality is similar to the CFP MSA hardware pin functionality. Fiber optic pigtails connect the transceiver to the system line card faceplate.

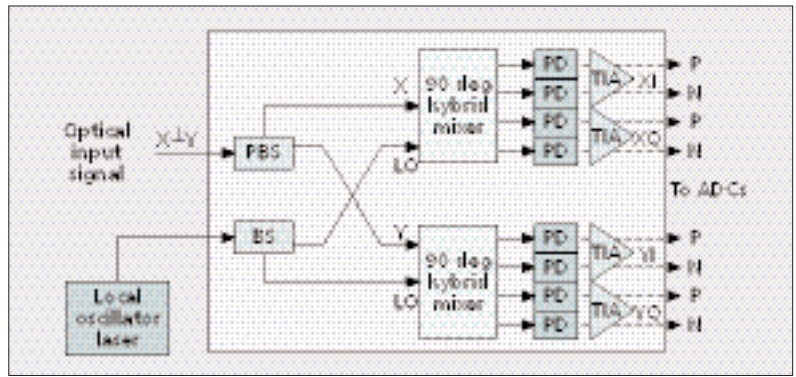


Figure 5. Functional architecture of a 32Gbaud DP intradyne coherent receiver.

The electrical interface IC(s) provide the SerDes and lane deskewing functionality necessary for adapting the host system signal frame format to the optical modulation format. The module electrical interface is generically specified in the OIF 100 G Module IA to allow vendor specific customization of multi-lane *M-lane* 11 Gb/s interfaces. Module electrical interfaces include but are not limited to the following:

- OTL4.10 — 10 lane for OTU4 [2]
- SFI-S — 10 lane + 1 de-skew [5]

The industry has been favoring OTL4.10 for the interface between the optical module and host system framer device as it is specifically designed to enable transport of 100GbE signals by mapping them into OTU4 of the OTN multiplexing structure and doesn't require an extra physical lane for deskewing such as in the SFI-S interface. Further details of the OTL4.10 interface rate and format specifications may be found in [2].

The transceiver interface IC may optionally implement soft decision forward error correction (SD-FEC) encoder/decoder functionality for improving OSNR performance in 100 G transmission. SD-FEC coding divides the signal level space into finer divisions for discriminating between a 1 or 0 bit and thus offers the potential of higher net coding gain than hard decision (HD) FEC which simply uses a single level for 1/0 bit discrimination. However, SD-FEC implementation requires increased coding processing bandwidth and performance, thus there is a trade-off between net coding gain improvement and implementation complexity/performance penalties. The OIF is currently assessing these trade-offs and preparing a whitepaper on the subject of FEC for 100 G DP-QPSK long distance transmission.

The IEEE MDIO/MDC interface ([1], Clause 45) has been adopted by OIF for module initialization, control, alarm and management communications. In addition to several advantages over alternative interfaces, such as 4MHz speed, deterministic response, required addressable memory space, and reliability, the MDIO has already been adopted for the client CFP module management. This enables implementation of a common module management hardware and software design for client and line-side transceiver modules in host systems.

The OIF 100 G Module Management Interface IA is currently in preparation and expected to be finalized before the end of 2010. Initial availability and deployment of the 100GbE CFP and OIF-compliant optical modules are anticipated for the late 2010–2011 timeframe.

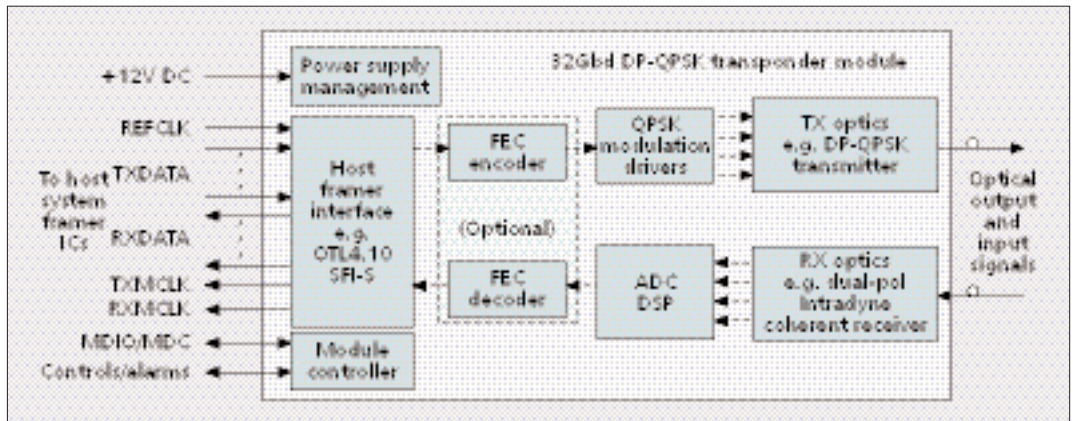


Figure 6. Functional architecture of the 32Gbuad DP-QPSK optical transceiver module.

Key features of the 100 G optical transceiver specified in the OIF 100 G Module IA are summarized as follows:

- Supports DP-QPSK modulation/coherent detection for data rates up to 32Gbuad, however, other modulation schemes not precluded
- 50 GHz DWDM optical transmission that is compatible with 10/40 Gb/s systems
- Host system interfaces: OTL4.10 (preferred), SFI-S
- Compact size: 5 × 7 supporting required thermal performance and sub-component physical layout
- Integrated heatsink or flat-top option for allowing heatsink customization
- Angular fiber exit ports positioned to enable flexibility in multi-port line card design
- 80W max power consumption at 70C max module case temperature
- Single +12 V DC power supply
- MDIO management interface
- 168-pin electrical interface supporting Tx/Rx data, power supply, MDIO/MDC, reference and monitoring clocks, programmable alarms and controls, LOS, Tx disable, low power mode, vendor specific functions and pins reserved for future use

SUMMARY AND NEXT STEPS

This article provided an overview and status of the 100 G Form-factor Pluggable (CFP) MSA and the OIF 100 G Transponder Module IA for 100GbE client interconnection and transport applications, respectively. At the time of this writing, the CFP MSA specifications were in the final stages of approval with expected public release in early 2010. The OIF 100 G Module and associated DP-QPSK transmitter and receiver module IAs were also in final stages of approval and expected to be released for public use in mid 2010. The OIF 100 G Module Management Interface IA is currently in preparation and expected to be finalized before the end of

2010. Initial availability and deployment of the 100GbE CFP and OIF-compliant optical modules are anticipated for the late 2010–2011 timeframe.

ACKNOWLEDGMENTS

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BIOGRAPHIES

JON ANDERSON (janderson@opnext.com) is Director of Technology Programs at Opnext, responsible for advanced technologies and standards development. Prior to joining Opnext in 2002, he was with Lucent Bell Laboratories where he held various technical staff and management positions and worked on optical technologies, network and systems architecture, advanced systems development and standards. He earned a Ph.D in Nuclear Engineering from MIT, a M.S in Mathematics from RPI, and a B.S. in Nuclear Engineering from Oregon State University. He is also Technical Editor of the OIF 100G Transponder Module IA.

MATTHEW TRAVERSO (mtraverso@opnext.com) is a graduate of Stanford University with degrees in Materials Science and Engineering. He is currently the Director of Strategic Marketing for Opnext, Inc. He has represented Opnext at various Standards Bodies, Multi-Source Agreements, and Technology Forums, and has written several articles on higher speed optical interfaces. He is also the editor for the "CFP MSA Hardware Specification."